Amendments to the Drawings:

A replacement sheet including a corrected Fig. 2D is attached hereto, in which reference numbers "44c" and "44d" are added. A marked up version of the sheet is also attached. The specification has previously been amended to refer to these reference numbers. No new matter is entered.

REMARKS

This is a response to the non-final Office Action dated August 25, 2004.

Regarding paragraph 1 of the Office Action and the objection to Fig. 2D, Applicant is submitting a revised Fig. 2D herewith as a replacement sheet. The specification has been previously been amended to refer to these reference numbers. No new matter is entered.

Claims 1, 3, 4, 10-12 and 14-21 are amended. Claims 2 and 5-9 are cancelled. Claim 13 is unchanged.

Applicant respectfully traverse the rejections to the claims under 35 U.S.C. §112.

Regarding claim 16, without conceding to the propriety of the objection, the claim is amended to refer to altering the coding rate of the rate matching circuit according to the bit deletion or repetition pattern.

Claims 1, 3, 4 and 10-21 have been rejected under 35 U.S.C. §112, second paragraph. Without conceding to the propriety of the rejection, the claims have been amended to refer to a bit "deletion or repetition" pattern.

Regarding claims 1 and 10, and the selection of a bit deletion or repetition pattern that ensures that the deleted or repeated bits are not required to enable all bits from the digital input signal to be reconstructed, note that this limitation is explained, e.g., in connection with Figs. 2c and 2d and page 7, line 23 – page 9, line 10 of the specification. As explained at page 8, lines 18-23, and referring to Fig. 2c, if every fourth bit is deleted or repeated when the block of data is read out, column by column, the result will be to delete or repeat four adjacent bits in the first and fifth rows. In contrast, the deletion or repetition pattern of Fig. 2d, where each column in the pattern or matrix is offset from the previous column, is advantageous because it avoids deleting

or repeating adjacent bits (pages 8-9, bridging sentence). This achieves the claimed goal of enabling all bits from the digital input to be reconstructed without the deleted or repeated bits. Regarding the assertion that the claimed limitation is not tied to any structural limitation, Applicant respectfully notes that claim 1 recites a rate matching circuit having means for selecting a rate matching pattern depending on the specified bit deletion or repetition pattern. Accordingly, the claimed limitation regarding the selection of the bit deletion or repetition pattern is clearly tied to the rate matching circuit (see blocks 18 and 28, Fig. 1).

Regarding claims 3 and 17, the rate matching pattern for each interleaved word is offset with respect to the rate matching pattern of the adjacent interleaved word or words. Fig. 2c clearly indicates an example of rate matching patterns, e.g., a pattern of 0's and 1's such as 100000100 and 010000010, that are offset as claimed. See page 8, line 24 – page 9, line 2. The degree of offset is specified as being with respect to the adjacent interleaved word or words.

Regarding claim 11 and 17, claim 11 recites that "the rate matching pattern forms a matrix including change bits", and claim 17 as amended recites that "said rate matching pattern includes change bits". Applicant respectfully submits that "change bits" are being introduced in these claims. There is no term such as "the" or "said" before "change bits" indicating an antecedent reference. Accordingly, there is no lack of antecedent basis.

Claim 11 is rejected under 35 U.S.C. §112, second paragraph as being incomplete for omitting a cooperative relationship for "change bits". Applicant notes that claim 11 sets forth that the change bits are part of a matrix that is formed by a rate matching pattern. The rate matching pattern is referred to in claim 1 as something that is selected by a means for selecting, which in turn is part of the claimed rate matching circuit. Accordingly, it is respectfully

submitted that there is a clear cooperative relationship between "change bits" and the structure of claim 1.

Regarding claim 12, the reference to the coding circuit having one of: (a) a fixed code rate, and (b) a predetermined number of rates for a variable data source, this claim does not recite that the coding circuit can have a fixed rate and a variable rate at the same time. Only one or the other is claimed, not both. Without conceding to the propriety of the rejection, the claim has been amended to provide further clarity.

Claim 12 is rejected under 35 U.S.C. §112, second paragraph as being incomplete for omitting a structural cooperative relationship between the coding circuit, fixed code rate, and a predetermined number of rates for a variable data source. Applicant notes that the "coding circuit" is a structural element, while the "fixed code rate" and "the predetermined number of rates for a variable data source" are characteristics, not structural components, of the "coding circuit". Accordingly, there can be no structural relationship between the "coding circuit" and its characterizing features.

Regarding claim 15, please see the comments above regarding claim 12.

Regarding claim 17, please see the comments above regarding claims 3 and 17 and the rate matching pattern, and the amended claim language which was made without conceding to the propriety of the rejection. In particular, the change bits are offset with respect to each other in the same way the rate matching pattern for each interleaved word is offset with respect to the rate matching pattern of the adjacent interleaved word or words. See Fig. 2c and page 8, line 24 – page 9, line 2. For example, in the rate matching patterns 100000100 and 010000010, the change bits are the 1's that are offset as claimed.

Regarding claims 18-20, the questioned claim language has been addressed above in regard to claims 11 and 17, and in the amended claim language, which was made without conceding to the propriety of the rejections.

In view of the above, the questioned claim language is believed to clearly meet the requirements of 35 U.S.C. §112, second paragraph. Withdrawal of the rejections is respectfully requested.

Claims 1, 3, 4 and 10-20 have been rejected under 35 USC 102(b) as being anticipated by Okumura et al. (Okumura). Okumura is concerned with a variable rate data transmission scheme that allows continuous transmission. To achieve this, a coded data sequence (output from the block "convolutional coder & interleaver", Fig. 1) is transformed into a QPSK symbol sequence with symbol rate R. A repetition code is then used to replicate the symbol sequence based on a rate index Q=Rm/R, where Rm is the maximum symbol rate (p.2026, col. 2, bottom). For example, Q=1, 2 or 4 (p.2027, col. 1, bottom). Thus, the symbol sequence can essentially be doubled or quadrupled. In contrast, Applicant's claim 1, for example, is concerned with adjusting the number of bits in a data block, which comprises a plurality of interleaved words, using a rate matching pattern that depends on an associated bit deletion or repetition pattern that is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from a digital input to be reconstructed. Thus, Applicant's invention is concerned with deleting or repeating bits in a data block. Okumura fails to disclose or suggest this feature since he is repeating the entire data symbol sequence that has been formed after coding of data block, e.g., using convolutional coding and interleaving, has occurred. Furthermore, Okumura is not concerned with using a rate matching pattern to achieve the goal of adjusting the number of bits in a data block. The repetition code of 1, -1 used by Okumura is not a rate matching pattern as

claimed because it is used for replicating an entire symbol sequence, not for adjusting the number of bits in a data block.

Withdrawal of the rejection is therefore respectfully requested.

Applicant's dependent claims similarly are patentable over Okumura.

For example, regarding claims 3 and 17, the spreading code used by Okumura is not analogous to Applicant's rate matching pattern, where the rate matching pattern for each interleaved word in a data block is offset with respect to the rate matching pattern of an adjacent interleaved word or words. This can be seen in that the spreading code, which is a CDMA spreading code, is applied to the data symbol sequence after the sequence is replicated (Okumura, Fig. 1). Thus, there is only one spreading code, not different rate matching patterns that are offset as claimed.

Independent claim 10, relating to a method that is an analog of the rate matching circuit of claim 1, is patentable over Okumura for the same reasons the rate matching circuit of claim 1 is patentable over Okumura.

Regarding claim 11, which depends on claim 1, as discussed above in connection with claim 1, the repetition code 1, -1 of Okumura is simply a multiplier used for repeating the entire data symbol sequence, but is not a rate matching pattern for achieving the goal of adjusting the number of bits in a data block as claimed. Even if the code 1, -1 could be thought of as a repetition pattern as asserted by the Examiner, this still does not provide a disclosure or suggestion of a rate matching pattern that forms a matrix including change bits as claimed that indicate a change of corresponding bits of interleaved words within a data block, wherein each row of the matrix includes a maximum of one of the change bits.

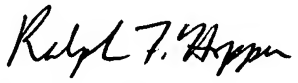
The remaining dependent claims are similarly patentable over Okumura.

Claim 21 has been rejected under 35 USC 103(a) as being anticipated by Okumura et al. (Okumura). Regarding the Examiner's assertion that it would have been obvious to form the data blocks as claimed, the Examiner is respectfully requested to provide a reference that supports this assertion.

Claims 1, 3, 4 and 10-21 have been rejected under the judicially created doctrine of double patenting in view of claims 1-19 of U.S. patent 6,671,851. Without conceding to the propriety of the rejection, Applicant will consider filing a terminal disclaimer at such time as is needed for the application to proceed to issuance.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,



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DATA INPUT: a_{11} a_{12} ---- a_{1k} a_{21} a_{22} ---- a_{2k} a_{31} a_{32} ---- a_{3k} ----

FIG. 2A

DATA INPUT: A_{11} A_{12} ---- A_{1n} A_{21} A_{22} ---- A_{2n} A_{31} A_{32} ---- A_{3n} ----

FIG. 2B

INTERLEAVING MATRIX

A_{11}	A_{12}	A_{13}	A_{14}
A_{15}	A_{16}	A_{17}	A_{18}
A_{21}	A_{22}	A_{23}	A_{24}
A_{25}	A_{26}	A_{27}	A_{28}
A_{31}	A_{32}	A_{33}	A_{34}
A_{35}	A_{36}	A_{37}	A_{38}
A_{41}	A_{42}	A_{43}	A_{44}
A_{45}	A_{46}	A_{47}	A_{48}

FIG. 2C

DELETION / REPETITION PATTERN

44a	44b	44c	44d
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0

FIG. 2D